CAN on Integration Technologies

CAN technology has reached the mature state where the powerful network technology is well covered by standard parts; mainly processors with integrated CAN periphery. Nevertheless every day, the CAN protocol is gaining access to new product segments where standard parts, mostly designed for automotive applications, have become inefficient or impossible. In this paper we will show you how CAN is used in application specific circuits and which market segments we serve.

The decision to own CAN technology on ASICs was made by INICORE in early 1992. Sulzer (Switzerland) decided to use CAN in their weaving machines, replacing lots of dedicated cables and mechanical synchronization with the real time capable CANbus. Since CAN was not yet so popular in automation at this time, CAN chips were difficult to get (for non-automotive applications) and expensive. For long-lived products like weaving machines, this risk was estimated to be too high. So Sulzer engaged INICORE for their proper CAN chip development. Today, these chips work in Sulzer's weaving machines, a market which represents about 0.5 billion dollars.

CAN on FPGAs and ASICs

INICORE was looking for a communication protocol, which fitted into the applications of our already well-defined customer base. Automation and telecommunication formed the main part of our integration projects, and we have found with CAN a protocol that has fulfilled the 3 most critical points:

1. Easy to integrate, no large memories, no software needed for basic operation.
2. Flexible, universal, fast and open layers.
3. Roadmap and support guaranteed for future applications.

CAN fulfilled all the criteria to great satisfaction and presented an optimal solution. Therefore, we invested again in CAN to bring the initial application to real IP.
A large amount of work has been invested to guarantee compatibility with the Bosch standard and already available chips. This insures correct operation in mixed networks.

Where we are today

The product of this major investment, implemented by means of our SA/SD methodology, brings the initial CAN application to real IP, and fulfills the strong needs for efficient IP based system design.

This product, called iniCAN, is built on structured, robust VHDL, test bench and documentation. It is ready to use and needs a minimal amount of support. Interfaces and the core context (interfaces, partitioning) fit perfectly in today's system designs. iniCAN works in simple standalone applications as well as in powerful communication modules.
This level of quality is needed to give confidence to customers, especially when CAN has been chosen for security reasons.

We are proud to bring CAN solutions to our customers. We have the ntellectual property that enables CAN functionality on system designs. Short turnaround times and minimized design risk insure the payback of the IP investment.

Products and applications

The CAN protocol has proved its advantages in a large range of applications. The iniCAN core represents optimum solutions for the following three segments:

1. *Low volume, highly specialized products:*

This segment is covered today by FPGA technology. The synchronous design style of iniCAN allows fast and predictable integration results in any of today's FPGA technologies, where gate count and speed areno longer limiting factors. Most limitations come from the physical package size of large FPGAs and cost. Typical applications are CAN test equipments, medical parts, individually designed nodes etc.

CAN on FPGAs enables you to see, bit by bit, what happens on the CAN bus. In addition to the valid CAN messages, you can also see bit error cases, error counters, internal status, frame position etc. without using a complete PC-based CAN analyzer tool. This is of interest for CAN network observations and error statistics in field applications.

The high flexibility of these solutions positions FPGA CAN nodes together with software based solutions (CPU + CAN).

The normally higher price per part of the FPGA is compensated for by the ease of use, where no programming know how and software maintenance is needed. Also, none of the standard chip suppliers will guarantee the long term availability of their products, particularly of special versions of processors.

CAN solutions based on FPGAs however, do not depend on a particular technology or version of a chip, since the circuit description is easily portable to any type of FPGA. There is always room for additional features, modifications and enhancements. Last but not least, the circuit is optimally protected against the copying of your particular product and know how.

FPGA prototyping is another important area where complex ASIC developments can be prototyped in hardware. This methodology gives you the guarantee that the same functionality will be available on a future ASIC design. Additionally, real system wide network simulations can be done with the FPGA based CAN nodes at low cost.

2. Mid volume applications:

The usage of standard CAN parts often has limitations such as size and power consumption. Further, the frequently required long term availability make its usage impossible or risky. The iniCAN offers, through the technology independent description, a long term availability and better performance through intelligent hardware support of higher layer functions. Combine CAN with your custom logic, DSP technology and peripherals all onto one chip!

An amazing example is the asCAN chip, where message routing, segmentation and reassembly of long frames, automatic configuration of each node etc. is supported by the chip, greatly reducing the interaction needed by the CPU. This chip even works standalone! The higher cost of the application specific parts are more than compensated for by better performance, product exclusivity and long term savings.

Integration technologies may change, but the data base remains the same. Migrations to newer versions of ASICs and FPGAs are efficient and can be done very fast.

In general, we can say that the need for an integration should come from the application, and not from the CAN interface. But mechanical constraints of miniaturized products can only be fulfilled with ASICs, where the smallest packages or even flip chip technology bring the size of the CAN interface down to a few square millimeters! Why not put CAN directly into cables or connectors?

Typical applications include advanced automation control, heavy machine industry, trains, miniaturized actors and sensors and intelligent mini motors.

3. High volume:

This segment is usually identified within the automotive industry, where standard parts have a nearly 100% coverage. Nevertheless, there are applications with special requirements where standard solutions are not applicable or do not exist yet. In this field, ASIC solutions win through lower price, the highest integration level and better performance. The growing acceptance of the CAN protocol opens up a wide range of applications, such as dedicated sensors and actors, multi CAN peripherals for RISC's and CPU's, network routers etc.

INICORE supports these three segments, being convinced that modern system design can no longer live without powerful FPGA prototyping, deep knowledge of advanced ASIC technology and competent application support. There is a gap today between trendy IP and final silicon. INICORE offers overall solutions and we support CAN technology from IP evaluation to the final ASIC volume production.

Application examples

The following two examples show how iniCAN is used in FPGA and ASIC technology:

1. IBM Boeblingen, Germany

IBM develops very highly integrated solutions for the automotive market. The goal was to design a powerful single chip system, where costly and space consuming external peripherals were completely eliminated. System-on-Chip solutions reduce cost and increase reliability. The tough time frame forced IBM to buy in ready to use CAN technology, rather than develop it with their own engineering crew. Another reason was to reduce the design risk by using an already-application-proved CAN core.

It was important to have the iniCAN core available in VHDL, in order to be able to synthesize it to any silicon, especially the chosen FPGA technology for prototyping and the final target ASIC technology. IBM mentioned that they had had good overall synthesis results on their tool environment without trouble. For time saving reasons, IBM had strong priorities on the 'ease of use' of the iniCAN core and well documented, simple interfaces. The gate complexity for the final ASIC product was second order.

"*We had an overall good experience with the iniCAN core*", said Dieter Staiger, Automotive_Embedded System Architect at IBM Germany. "*For future IP acquisition, we would insist even more on proven design results, also for the very important task of FPGA prototyping*."

2. Lucas Automotive Electronics, UK

Lucas Varity, Birmingham, develops car electronics, where CAN is, or will be part of nearly every subsystem. Innovative solutions in future applications require robust, high density electronics at the lowest cost. Therefore, the use of integration technologies is often the only way to fulfill all these requirements. ASIC technology is used anyway in the product, implementing CAN on the same chip is the most efficient option. This solution allowed the system to be kept as small as possible, reducing the number of parts and increase reliability. “We have better control of message filtering and processing”, said Mark Bowen, principal engineer. This way, the interrupt load, communication support etc. can be adapted to the needs of the specific application, which leads to better system performance and the generally lower cost of the integrated CAN functionality.
Flexibility of the ASIC vendor choice makes the use of VHDL a must, so Lucas Varity looked for synthesizable CAN IP. Since VHDL represents the standard entry mechanism for ASIC development at Lucas Varity, the iniCAN fits into their environment perfectly. Using CAN as a pre-verified part, which is ready to use, helps to limit the engineering resources and to keep them on a project relevant task, in order to guarantee the tough time frames and reduce the developmental cost. The standard CAN functionality was bought in from INICORE, which greatly supported the progress of this ambitious project.

The SD document, which describes the operation of the iniCAN core in full detail, ensures long term availability and efficient further usage of the IP investment.

CAN-ASICs only for experts?

One may think that integrated solutions with CAN could only be utilized by big companies like the ones mentioned above, which have their own ASIC development crew. This is partially true. The usage of CAN in integrated, customized solutions requires experts for conceptualization, prototyping and ASIC implementation.

But INICORE, acting as a system design house, can offer this service together with the needed CAN cores. We support projects from the very beginning and bring in our experience already at the concept level of the project. An optimized message filter architecture reduces the heavy interrupt load for the CPU at high bit rates, which gives you more performance for the application program. Problems like the priority inversion can be solved in an elegant way without the interaction of the processor. The number of masks in the message filter can be adapted to insure data throughput. Combining masks with FIFOs avoids data loss and time stamping watches over the real time capability.
It is obvious that this kind of message filter cannot be designed for a couple of hundred FPGAs or ASICs. But in advanced

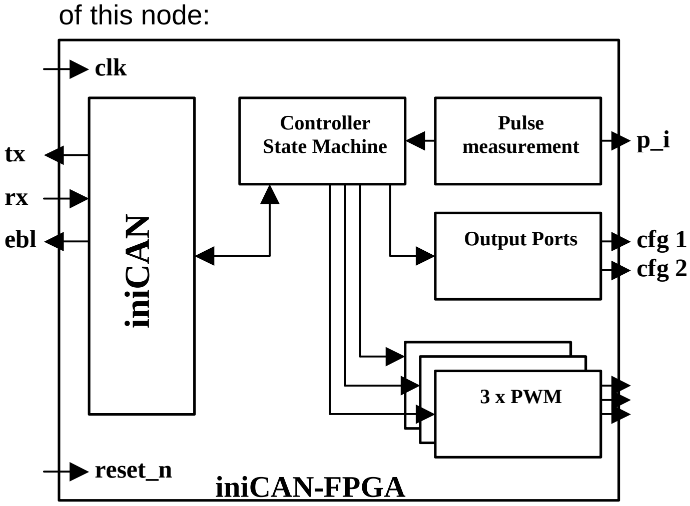
applications, the overall system cost can be substantially reduced.

Remote IOs on FPGAs

Remote IOs on FPGAs compete directly with software based solutions. Both of them are flexible and competitive. The application requirements, the company knowledge in microelectronics and software, the number of parts per application etc. decide which solution is the best in terms of cost and performance. Lower volume projects are not dominated by the parts price! FPGAs with your particular functionality can be designed for you and be used like standard chips, say programmed and tested. No experts are needed for programming. You focus on the company's key technology rather than how to implement CAN networking details, study hundreds of pages in data books etc.

The following example shows how a simple remote IO node could look:

In a machine, using CAN2.0B at 1 Mbit/s, you have to measure the sporadic pulse lengths of a sensor output. 2 control bits for configuration and a triple PWM with 12 bits resolution at 8kHz are also needed. There are a few more functions needed, such as control logic for other chips, a clock divider etc. The possibility of including all that into one FPGA reduces the overall size of the node by making space consuming external components (except the CANbus driver) obsolete.
The following picture shows a block diagram of this node:



While the iniCAN is handling the CAN protocol, the 'Controller State Machine' decodes the incoming CAN messages and routes the data to the 'Output Ports' or one of the 'PWMs'. Moreover, when a pulse has been detected by the 'Pulse Measurement' unit, a message is generated and sent over the CAN bus.
The node address, group code or functional identification can be coded by parallel inputs.
Physically, such CAN components can be realized e.g. in ACTEL devices, where no external programming ROM is needed and the chip is immediately functional after reset. Furthermore, your device is fully protected and 100% under your control, which means short delivery times, guaranteed availability and the possibility to modify the chip for special applications, future needs etc.

If we compare this solution to CAN-CPUs, you may say that you can have all that at lower price. Actually, this can be the case. The goal of customized solutions is not replacing existing, optimized standard parts, but offering solutions for special requirements. Standard components rarely have the peripheral components and performance you need. Examples are the number of IOs, the resolution, speed and number of PWM's, no pulse width measurement (or not the needed performance when you do it in software). Conditions like these often push hardware designers to choose a chip with a too high performance, in order to reach the goal in one particular case. Others use additional components to realize the missing peripheral units. In projects like this, the commercial calculation is often reduced to parts price, which does not reflect the real production cost. Assembly, stock handling, the reduction of reliability, the more expensive test procedure, the increased size and power consumption (power supply!) etc. are often not included in price calculations. And it is just there, where dedicated solutions win!

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