INICORE
System-on-Chip from Spec to Silicon

Optimized for

Actel

iniCPU

Description

The iniCPU, a 8-bit microprocessor, implements one of the most powerful 8-bit instruction sets, the one of the 6809. This CPU supports several different addressing modes as well as position independent code.

The iniCPU is software compatible to the original 6809. It implements the same instruction set, interrupts and the behavior of all flags is the same. Due to advanced design techniques, the code execution is faster than the original. Additional acceleration can be achieved by using a fast FPGA such as one of the Actel AX family.

This core is designed for embedded systems where the CPU together with peripheral functions such as timer, UART, interrupt controller, GPIO interface and watchdog are all integrated on the same chip. A synchronous local bus interface facilitates interfacing to several modules. This interface even supports multi-master applications where more than one CPU or a DMA unit accelerates system performance.

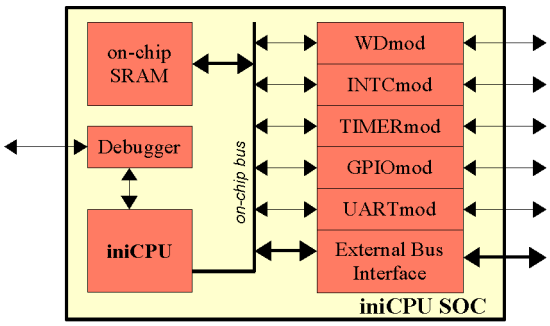

Figure 1: Sample System-on-Chip Application

For evaluation and debugging, a demonstration board is available that shows the functionality of the iniCPU in a hardware testbed. The demonstration board shows the iniCPU with peripheral logic in an Actel ProASIC[PLUS] device.

Features

- 8-bit microprocessor
- 6809 software compatible
- Save operation, illegal opcode recognition
- Supported by 3rd party compiler and assembler
- Address expansion circuit (page mode)
- Designed for system embedding
- Synchronous system bus interface
- Full synchronous design

Applications

- Obsolete 6809 replacement
- Enhanced 6809 systems
- 8-bit System-on-Chip

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
ProASIC[PLUS]	APA150			2789		45%
Axcelerator	AX500-3	336	1593			24%
SXA	SX32A-3	340	1519			65%

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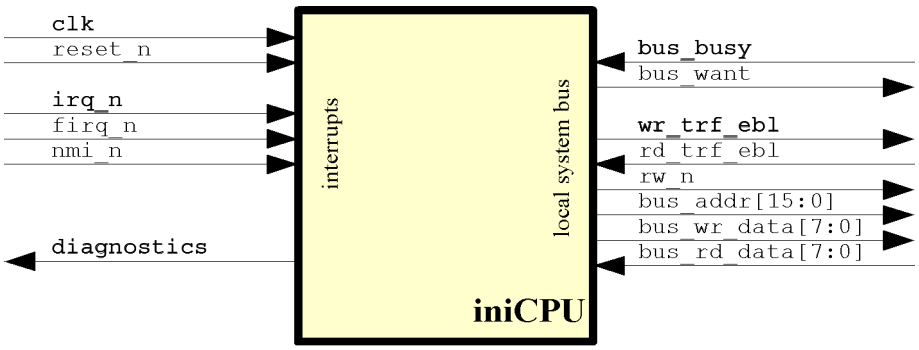

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
Interrupts		
irq_n	in	Interrupt request, active low
firq_n	in	Fast interrupt request, active low
nmi_n	in	Non maskable interrupt request, active low
Local Bus Interface		
bus_want	out	CPU bus request
bus_busy	in	Local bus status
bus_addr [15:0]	in	Address bus
bus_rd_data[7:0]	in	Read data bus
bus_wr_data[7:0]	out	Write data bus
wr_trf_ebl	out	Write transfer enable
rd_trf_ebl	out	Read transfer enable
rw_n	out	Read / write not
Diagnostics		
mem_rdy	out	Internal memory ready
seq_state[5:0]	out	Command sequencer state
cc[7:0]	out	Condition code register
pc[15:0]	out	Program counter
stack[15:0]	out	Stack pointer
stack_operation	out	Stack operation, active high
opcode[5:0]	out	Operation code

Implementation

The core is either available in VHDL or Verilog. The design is fully synchronous and can be target to any technology. The RTL source code is accompanied with a self verifying testbench that verifies every instruction code and addressing mode, interrupt sources, arithmetic results and status flags.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

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