INICORE
System-on-Chip from Spec to Silicon

Optimized for Actel

TIMERmodule

Description

The TIMERmodule is part of Inicore's IPmodule family. Timer and counters are essential in CPU applications. Used to count events, measure time intervals or frequencies, or generate periodic timing events.

The TIMERmodule provides two independent 16-bit timers each with its own 16-bit pre-scaler. An additional pre-scaler is provided for applications where external high frequency events or clocks control the operation.

The two timers can be locked for measurements over a given time span. Timer B provides the observation window while Timer A is counting events.

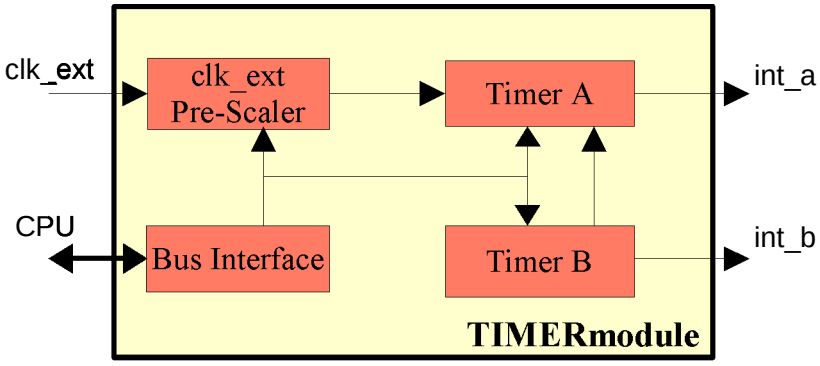

Figure 1: Block diagram

The operating mode of each timer can be selected independently:

- Free running: Timer is reloaded with initial value after counter reaches zero
- One-shot: Timer stops after reaching terminal count
- Window mode: Timer A counts while Timer B generates observation window

Each timer generates an interrupt upon arriving at terminal count zero. A count capture command is available to sample the current count state without interrupting the timer.

Features

- Clock prescaler for external high frequency sources
- Internal or external clock source select
- Supports single-shot, free running and counter mode
- Provides two 16-bit counter /timers with individual 16-bit prescalers
- Two interrupt sources, one for each counter/timer
- Individual counter capture commands
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Gate-count optimization
  - Configurable CPU readback path

Applications

- Industrial control
- CPU subsystems
- System-on-Chip design
- Watchdog or timing reference

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
ProASIC[PLUS]	APA150			1216		20%
Axcelerator	AX500-3	170	292			5%
SXA	SX32A-3	170	297			16%
eX	EX256	170	297			58%

INICORE INC. 5600 Mowry School Road Suite 180 Newark, CA 94560 Tel: 510 445 1529 Fax: 510 656 0995 www.inicore.com

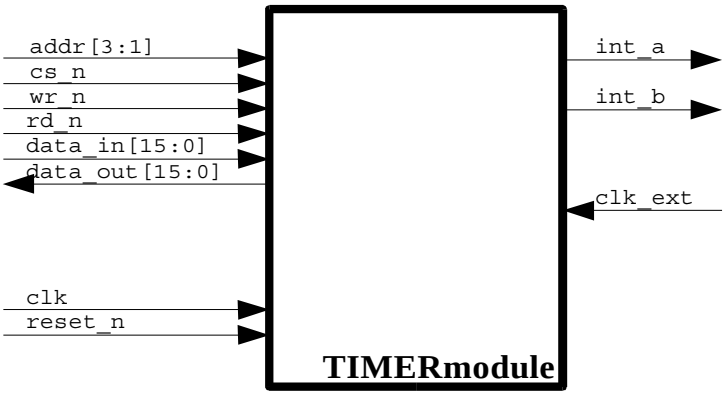

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[3:1]	in	Address bus input
data_in[15:0]	in	Data bus input
data_out [15:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
Timer		
int_a	out	Interrupt request
int_b	in	Interrupt source requests
clk_ext		

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. Synthesis options are included to use the core in 8, 16 and 32-bit systems.

With a separate APB wrapper, the core can be used in ARM subsystems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

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